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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,646	12/27/2001	Mark Randolph	G0727/2243P	5662

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09/29/2003

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EXAMINER

LOKE, STEVEN HO YIN

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 09/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/032,646

Applicant(s)

RANDOLPH, MARK

Examiner

Steven Loke

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) 4-10 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-15 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 17-25 is/are rejected.
- 7) ☒ Claim(s) 16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

1. Claims 1, 16 and 25 are objected to because of the following informalities: Claim 1, line 10, the phrase "the N-type junction" has no antecedent basis. Claim 16, line 1, the phrase "the p-type regions" and line 3, the phrase "the first n-type regions" have no antecedent basis. Claim 25, lines 2-3, the phrase "the plurality of source regions" has no antecedent basis. Appropriate correction is required.

2. Claims 19-25 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses a fifth n-type region of substrate disposed adjacent to the first and forth regions, and a sixth n-type region of substrate disposed adjacent to the second and third regions, the fifth and sixth n-type regions including p-type dopants at a concentration corresponding to the first and second p-type regions as claimed in claim 19.

Figs. 2, 4 and 5C disclose the compensated n-type regions [44] including a p-type dopant at a first predetermined concentration formed between the p-type regions of two rows of memory cells. The specification never discloses a plurality of compensated n-type regions of substrate disposed between the p-type regions within a row of memory cells, the compensated n-type regions including a p-type dopant at a first predetermined concentration as claimed in claim 20.

Fig. 2 discloses a Vss contact [30] for a plurality of source regions. The specification never discloses a plurality of electrical contacts, each electrical contact coupled to a corresponding one of the plurality of source regions as claimed in claim 25.

3. Claims 1-3, 17-19, 24 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 10, the phrase "the N-type junction" is unclear as to how a junction formed by N-type impurity. Is it being referred to an n-type region?

Claim 17, lines 4-5, the phrase "forth side" is unclear as to what is it meant. Is it being referred to the "fourth side"?

Claim 17, line 6, the phrase "a forth n-type region" is unclear as to what is it meant. Is it being referred to the "fourth n-type region"?

Claim 17, line 6, the phrase "a forth n-type region of substrate disposed adjacent to the third and forth regions" is unclear as to how a fourth n-type region of substrate disposed adjacent to the third and fourth regions.

Claim 19, line 2, the phrase "first and forth regions" is unclear as to what is it meant. Is it being referred to the "first and fourth regions"?

Since claim 23 and fig. 2 disclose only one source region comprises alternating n-type regions and compensated n-type regions for every two rows of memory cells, it is unclear why claim 24 discloses more than one source region in the semiconductor memory.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Komori et al.

In regards to claim 1, Komori et al. show all the elements of the claimed invention in figs. 2, 3A-3C and 4A-4M. It is a semiconductor device, comprising: a substrate [10]; a row of transistors [Q] disposed on the substrate, each transistor having a stacked gate structure [18, 22] and a drain [24]; wherein adjacent transistors [Q] are isolated from each other by P-type regions [28] of the substrate; a layer of polysilicon [22] interconnecting the transistors in the row; and a source region [24, 37] comprising an N-type region of the substrate adjacent to row of transistors and having a contact [38] coupled thereto, wherein the N-type region [24, 37] includes a plurality of P-type regions (the p-type regions [12] originally formed under the contact [38] and between the n-type source regions [24]) that have been over-doped to form N-type regions, and wherein the N-type region extends across the source region to provide a planar electrical path between the drains [24] of the transistors and the contact [38]. It is inherent that the planar electrical path reduces the resistance of the source region.

In regards to claim 2, Komori et al. further disclose the transistors are located in core regions of the substrate [10].

In regards to claim 3, Komori et al. further disclose the transistors are located over active areas in the substrate, and the active areas include N-type regions [24, 37].

6. Applicant's arguments filed 7/2/03 have been fully considered but they are not persuasive.

It is urged, in page 8 of the remarks, that Komori does not show that the source region includes areas in which a p-type semiconductor has been over-doped to form an n-type semiconductor as required by claim 1. However, as mentioned in the rejection, the N-type source region [24, 37] includes a plurality of P-type regions (the p-type regions [12] originally formed under the contact [38] and between the n-type source regions [24]) that have been over-doped to form N-type regions.

It is urged, in page 9 of the remarks, that Komori never discloses the N-type junction extends across the source region to provide a planar electrical path. However, fig. 3C of Komori shows an n-type region [24, 37] extends across the source region [24, 37] to provide a planar electrical path. The contact [38] can also make by n-type silicon (col. 6, lines 39-41).

7. Claims 11-15 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: The major difference in the claims not found in the prior art of record is a second n-type region of substrate disposed adjacent to the first and second regions, the second n-type region including p-type dopants at a concentration corresponding to the first p-type region.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

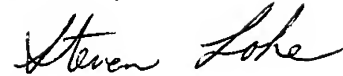
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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September 24, 2003

Steven Loh
Primary Examiner

A handwritten signature in cursive script that reads "Steven Loh".